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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,633	02/11/2002	Michael A. Todd	ASMEX.328A	7137

20995 7590 07/09/2004

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EXAMINER

PHAM, LONG

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/074,633

Applicant(s)

TODD, MICHAEL A.

Examiner

Long Pham

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) 19-35 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 6-18 is/are rejected.
- 7) ☒ Claim(s) 3-5 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date see attachment.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species I (claims 1-18) in the reply filed on 04/26/04 is acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Ueda et al. (US 6,090,666) or Pomerode et al. (US 2002/017130) or Yamazaki et al (US 2004/0115953).

With respect to claims 1 and 2, AAPA teaches a deposition method comprising (see figures 1A-1C and the Background of the Invention on pages 1-3 of this application):

providing a substrate 100 disposed within a chamber, wherein the substrate comprises a first surface 120 having a first morphology of single crystalline and a second surface 110 having a second surface morphology different from the first surface morphology;

introducing silane into the chamber under chemical vapor deposition conditions; and

depositing a Si-containing film onto the substrate over both the first surface and the second surface.

However, AAPA teaches introducing silane into the chamber to form the Si-containing film but fails to teach introducing trisilane instead of silane into the chamber to form the Si-containing film.

Ueda et al. teach introducing trisilane into a chamber to form a Si-containing film having spherical semiconductor nanocrystals uniform in size and shape. See col. 6, line 60 to col. 7, line 20.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use trisilane in the method of AAPA to achieve the above benefit.

Alternatively, both Pomerede et al. and Yamazaki et al. teach depositing a Si-containing film by using trisilane source. See [0076] of Pomerede et al. and [0044] of Yamazaki et al.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use trisilane in the method of AAPA because that allows formation of a Si-containing film.

With respect to claim 6, AAPA further teaches the first surface comprises of a semiconductor material and the second surface comprises of a dielectric material. see figures 1A-1C and the Background of the Invention on pages 1-3 of this application.

With respect to claim 7, AAPA further teaches the semiconductor material comprises of silicon but fails to teach that semiconductor material comprises boron or arsenic.

However, the use of boron or arsenic doped semiconductor material is well-known in the semiconductor art.

With respect to claim 8, AAPA further teaches the dielectric material comprises of silicon dioxide. see figures 1A-1C and the Background of the Invention on pages 1-3 of this application.

With respect to claim 9, AAPA fails to teach that the Si-containing film is a silicon buffer layer.

However, the use of silicon as buffer film is well-known in the semiconductor art.

AAPA further fails to teach the range for the thickness of the buffer layer.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the thickness of the buffer layer through routine experimentation and optimization to obtain optimal or desired device performance because the thickness of the buffer layer is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claims 10 and 11, AAPA in combination with Ueda et al. further teach forming a SiGe film using a germanium source and a silicon source of trisilane. See col. 6, line 60 to col. 7, line 20.

With respect to claim 12, since AAPA in combination with Ueda et al. teach the first and second surfaces having different morphologies, at least a portion of the first surface would inherent be non-coplanar with the second surface.

With respect to claim 14, AAPA fails to teach the range for the deposition temperature.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the deposition temperature layer through routine experimentation and optimization to obtain optimal or desired device performance because the deposition temperature is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 13, 15, and 16, since AAPA in combination with Ueda et al. teach a claimed process, the Si-containing film would inherently have a first thickness over the first surface and a second thickness over the second surface.

AAPA in combination with Ueda et al. fail to teach the relative thicknesses between the first and second thicknesses.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal relative thicknesses between the first and second thicknesses through routine experimentation and optimization to obtain optimal or desired device performance because the relative thicknesses are result-effective variables and there is no evidence indicating that they are critical or produce any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 17, the formation of a in situ doped Si-containing film is well-known in the semiconductor art.

With respect to claim 18, since AAPA in combination with Ueda et al. teach the claimed process, a crystalline morphology of the Si-containing film would be formed over the first surface and a non-crystalline morphology the Si-containing film would be inherently formed over the second surface.

Allowable Subject Matter

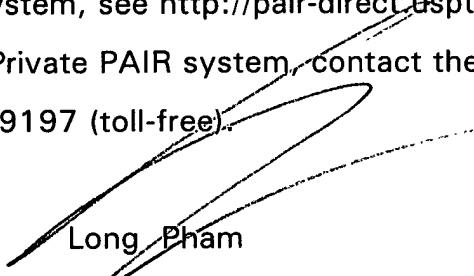
3. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Long Pham
Primary Examiner

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